AMENDMENTS TO THE CLAIMS

1-19. (cancelled)

20. (original) A method for implementing delay locked loop in an integrated circuit device, the method comprising:

configuring a coarse delay chain in series with a micro-stepped delay chain;

said coarse delay chain including a plurality of coarse delay units configured for selectively providing a coarse delay with respect to an input clock signal, and said micro-stepped delay chain configured for selectively providing a fine delay adjustment with respect to said input clock signal; and

configuring a plurality of parallel signal paths within said micro-stepped delay chain, wherein one or more of said parallel signal paths are capacitively loaded so as to provide said fine delay adjustment.

21. (new) The method of claim 20, wherein:

a first of said plurality of parallel signal paths comprises a single coarse delay unit;

a second of said plurality of parallel signal paths comprises a pair of coarse delay units; and

the remainder of said plurality of parallel signal paths each comprising a single coarse delay unit having an intermediate node thereof loaded with a stepped value of capacitance with respect to one another;

wherein a signal propagated through any of said remainder of said plurality of parallel signal paths has a delay associated therewith that represents a stepped valued of delay between the delay provided by said single coarse delay unit and the delay provided by said pair of coarse delay units.

22. (new) The method of claim 21, wherein said single coarse delay unit comprises a pair of serially connected NAND gates.

23. (new) The method of claim 21, further comprising:

coupling an input signal to the micro-stepped delay chain to input terminals of each of said parallel signal paths; and

coupling a micro-stepping control signal to said single coarse delay unit and said capacitively loaded single coarse delay units;

wherein said micro-stepping control signal is further configured such that only one of said single coarse delay unit and said capacitively loaded single coarse delay units are enabled at a given time.

24. (new) The method of claim 23, wherein said micro-stepped delay chain further comprises an OR gate, said OR gate having each of said plurality of parallel signal paths as inputs thereto.

25. (new) The method of claim 24, wherein said pair of coarse delay units is biased in an enabled state such that a maximum delay of a signal propagated through said micro-stepped delay chain is the delay provided by said pair of coarse delay units.

26. (new) The method of claim 22, wherein said pair of serially connected NAND gates comprise equalized NAND gates.

27. (new) The method of claim 20, wherein said coarse delay chain further comprises:

a plurality of serially connected coarse delay stages, each of said plurality of coarse delay stages configured to selectively provide a discrete number of coarse delay values, wherein the delay value of said discrete number of coarse delay values is successively larger for each successive coarse delay stage.

28. (new) The method of claim 27, wherein said coarse delay stages are configured such that discrete number of coarse delay values are implemented by routing an input signal through a specific number of said coarse delay units included within said coarse delay stages.

29. (new) The method of claim 28, wherein said discrete number of coarse delay values are selected through a multiplexing device.

30. (new) The method of claim 29, wherein at least a portion of said multiplexing device is configured from one of said coarse delay units.

31. (new) The method of claim 28, wherein each of said coarse delay units comprises a pair of serially connected, NAND gates.

32. (new) The method of claim 31, wherein said pair of serially connected NAND gates comprise equalized NAND gates.

33. (new) A method for implementing a micro-stepped delay chain for use in a delay locked loop, the method comprising:

coupling a plurality of parallel signal paths to a common input;

a first of said plurality of parallel signal paths comprising a single coarse delay unit;

a second of said plurality of parallel signal paths comprising a pair of coarse delay units; and

the remainder of said plurality of parallel signal paths each comprising a single coarse delay unit having an intermediate node thereof loaded with a stepped value of capacitance with respect to one another;

wherein a signal propagated through any of said remainder of said plurality

of parallel signal paths has a delay associated therewith that represents a stepped valued of delay between the delay provided by said single coarse delay unit and the delay provided by said pair of coarse delay units.

34. (new) The method of claim 33, wherein each of said coarse delay units comprises a pair of serially connected NAND gates.

35. (new) The method of claim 33, further comprising:

coupling a micro-stepping control signal to said single coarse delay unit and said capacitively loaded single coarse delay units;

wherein said micro-stepping control signal is further configured such that only one of said single coarse delay unit and said capacitively loaded single coarse delay units are enabled at a given time.

36. (new) The method of claim 35, further comprising configuring an OR gate having each of said plurality of parallel signal paths as inputs thereto.

37. (new) The method of claim 36, wherein said pair of coarse delay units is biased in an enabled state such that a maximum delay of a signal propagated through the micro-stepped delay chain is the delay provided by said pair of coarse delay units.

38. (new) The method of claim 36, wherein said pair of coarse delay units is biased in an enabled state such that a maximum delay of a signal propagated through the micro-stepped delay chain is the delay provided by said pair of coarse delay units.